DRAFT ONLY

Document Ref: ISB-2/0
(i.e. Document ISB-1/1 May 1980, extensively rewritten)

Issue: 0

Date: October 1988

ISBUS-2. INTERAK BACKBOARD

USER MANUAL - ISSUE 0

Manual Price £1.50

PREFACE

This was the very card produced especially for the Interak 1 computer, although at the time there were no Interak Cards.

All of the computer cards available at that time were manufactured by the firm Kemitron Electronics Ltd., (which is still very much in existence, and specialises in Industrial and Scientific Assembled Computer Systems).

The fundamental difference between the Kemitron Bus and ISBUS is that the Kemitron Bus (or K-Bus for short) is used only with 43-way single sided edge connectors, and ISBUS is planned to use double sided connectors i.e. 86-way. (To be pedantic subtract one from each side for the polarisation slot.)

As the two sides of the circuit boards used are referred to as "A" and "B", the name "ISBUS-A" has been given to the 43-way bus (which approximates to the K-Bus) and the name "ISBUS-B" has been given to the 86-way bus which uses the "B" connections as well.

The acronym ISBUS stands for "International Card Size Standard Bus". The International Card Size referred to here is 8" long and 4.5" wide, i.e. the natural size to fit into a standard 3U 19" Rack. Two main suppliers of International Card accessories are RS Components Ltd. and Vero Electronics Ltd., although your Interak Supplier will also have suitable hardware at competitive prices.

Great care has been taken to organise things so that ISBUS-B does not render ISBUS-A obsolete. Full details will be given in this document but for now it will be sufficient to note that ISBUS-A is basically a 16-address line bus (i.e. 64K) and ISBUS-B increases the number of address lines to 24 (i.e. 16 Megabytes of address space). Things have been carefully organised so that a small 64K system can be run "within" the larger 16M, without the memory contention problems which would normally prevent simple expansion. (Kemitron Ltd. use a different method to expand past 64K: they use a method of "bank" switching to allow access to more than 64K on their existing 16-bit bus. The technique will not be discussed much here as ISBUS-B uses extra address lines instead.)

In summary ISBUS is the name given both to the physical printed circuit board and to the specification detailing what the signals on the various tracks should be.

ERRATA

~~Issue 5 Mar 1983~~

CONTENTS

(Total number of pages Issue 0 Manual: 26)

** = not written yet, - purchasers of manual will receive - Issue 1 F.O.C. when completed.

ISBUS BACKBOARD GENERAL FEATURES

* Epoxy Glass, Tinned.
* Solder Resist on both sides.
* Component Ident on both sides.
* Drilled for Both ISBUS-A (Single-sided) and ISBUS-B (Double-sided) edge connectors and Power Connectors.
* INTERAK 1 Compatible (and Beyond).
* Double Sided, All Tracks Visible, (and thus Repairable).
* Low Cost.
* Provision for Multiple Power Supplies (0V, +5V, +12V, -12V).
* Provision for connecting power via Plugs and Sockets.
* Includes 3 "Daisy Chain" Lines for Future Enhancements, or for Present Users' Experiments.
* Suits International Size Cards (4.5" x 8")
* Fits 19" Rack, with Space for Power Supply at One End.
* Insertion Force of Plug in Cards is Transmitted to Rack Metalwork Directly, to Avoid Flexing the ISBUS Backboard Itself.
* Dimensions 4.4" x 12.9"
* Space for 13 Cards on 1" Centres.
* No manufacturer's name appears on the card, thus ideal for OEM (Original Equipment Manufacturer) use.

DESCRIPTION

The ISBUS backboard is used to interconnect all the INTERAK 1 cards. The ISBUS allocations are in two forms: ISBUS-A, which defines the signals on the A-side 43-way connector used for the cards, and ISBUS-B. ISBUS-B defines the signals on the B-side 43-way connector. Such refinements as an extra 8 address lines, and an extra 8 data lines, interrupts and the like. Previously, the main decision a user had to make was whether or not to go for single or double sided connectors. Luckily this is no longer a problem: the double sided connector is so popular that its price (when purchased from Interak suppliers) has dropped below that of the single sided connector which is thus pointless to continue to stock.

Mounting

The ISBUS backboard is fitted towards the left-hand side of a 19" card frame (viewed from the front). This leaves a generous amount of space to the right for the user to fit a couple of 3.5" disk drives.

The power supply can be mounted at the rear of the ISBUS backboard as detailed in the PSU manual. For safety the mains voltage is taken directly to the power supply, and only the low voltages are taken to the ISBUS board.

Power Supplies

The power supply tracks are much broader than those used for signals and the +5 volt and 0 volt rails (the major power use in most systems) are also reinforced by additional copper tracks on the 'B' side. For maximum reliability the power rail connections are made using three 0.156" power connectors, soldered onto the ISBUS board at the positions indicated in the construction section of the manual.

Mechanically Rigid

The ISBUS board is used solely for interconnecting the edge connectors, and is not used for their mechanical support. The edge connectors are each bolted into the rack directly, so that the rack takes the force when cards are plugged in and out. Often the system of plug in cards is criticised unfairly for being unreliable, when in fact it is the design which is wrong. There is a popular cheap computer on the market which has a rear mounted plug in memory expansion which is notorious for unreliability, but the cause is quite simply the lack of mechanical support - the edge connector should not serve this purpose as well as make the interconnections.

The method used for mounting the ISBUS means that it is not constantly being flexed back and forth when cards are plugged in and out. This is important as the tiny copper tracks could easily develop hairline fractures if subjected to such abuse, causing intermittent faults

which are the world's worst in a computer.

The ISBUS assembly comprises the fibreglass printed wiring board and the connectors soldered to it. Any stress applied to the connector is transmitted via the connector mounting brackets to the card frame. The printed wiring board in this way is protected from stress. This keeps the risk of broken solder joints/tracks and intermittent faults to a minimum.

The backboard assembly should not really be used without a card frame as this would put stress onto either the ISBUS board or the connectors, increasing the risk of intermittent faults and unreliable operation. When constructed as described in this manual, ISBUS and its connectors form a highly reliable assembly.

Power supplies are connected to the Bus using suitable heavy gauge connecting cables/wires. The connections are made via power connectors on the ISBUS board itself.

The ISBUS assembly is used to interconnect the circuit boards used in the Interak System; via the connectors it is bolted onto the back rails of the Card Frame (Rack), and the circuit boards slide on runners so that they plug directly into the mounted edge connectors.

ISBUS Signal Description.

A list of bus allocations can be found in the diagram section of this manual. The function of each signal/bus line will be described in this section.

Signal names which begin with an 'N' indicates that the signal is active low. Signals named without the 'N' are active high. Note that 31A on connector 1 is connected to 30A on connector 2, 31A on connector 2 is connected to 30A on connector 3 and so on, similarly for the other 'daisy-chain' signals on the 'B' side of the connector31B to 30B and 32B to 33B.

"A" Side Connectors

1A NIOREQ I/O Request (TTL Level Output from CPU/Controller)

Input/Output request line. Active low. Indicates that the address bus lines AB0 to AB7 hold a valid address for an I/O access. (During an interrupt acknowledge cycle, and only then, NIORQ is produced at the same time as NM1(OCF); at all other times NM1(OCF) is produced together with NMREQ or NEMREQ, never with NIOREQ.)

The 8 address bits define which one of 256 ports are to be accessed. Future systems may have a larger I/O port space, and to prevent these ports conflicting with the existing 256 ports

NIOREQ will be denied to the bus; instead an "extended I/O request" signal will be produced.

2A NMREQ Memory Request (TTL Level Output from CPU/Controller)

Memory request line, active low; indicates that the 16-bit address bus, AB0-AB15, holds a valid address for a memory access, ie an access to one of the first 64K memory addresses is in progress.

Future systems will have a further 8 address lines (AB16-AB23), defining a 16 Megabyte memory space. To prevent the addresses in the larger space conflicting with the existing 64K space NMREQ will be denied to the bus; instead an "extended memory request" signal will be produced.

3A NWDS Write Data Strobe (TTL Level Output from CPU/Controller)

Write line, active low. Indicates that the data bus has valid data to be written to a memory location or output to an I/O device.

4A NRDS Read Data Strobe (TTL Level Output from CPU/Controller)

Read Line, active low. Indicates that the CPU/Controller wants to read data from a memory location or I/O device.

5A-20A AB15-AB0 16-bit Address Bus (TTL Level Outputs from CPU/Controller)

These are the address lines for a normal memory access (ie when NMREQ or NEMREQ are present). The positive logic convention is used, i.e. a "0" is represented by a low voltage and a "1" by a more postive voltage. The address lines are usually driven from the CPU, but if the CPU card can be rendered high impedance (disabled) these lines can be driven from other controllers (e.g. Direct Memory Access (DMA) devices). In ISBUS "A" systems these 16 are all that are used , but in ISBUS "B" systems there are a further 8 lines (AB16-AB23) defined for addresses.

When the access is to the I/O space (ie when NIOREQ or NEIOREQ are present) the lower 8 lines, AB7-AB0, carry the address of the I/O port being accessed and the other lines carry information which depends on the particular microprocessor in use.

A final use of the address bus is to carry a "refresh address" for dynamic RAMs. This is issued at a time when the MPU is not using the bus (ie immediately after an opcode fetch, while the instruction the opcode represents is being decoded) and allows an easy refresh of dynamic RAMs. The indication that the address bus bears a refresh address is provided by the NRFSH signal.

NMREQ and/or NEMREQ are also present but NRDS and NWDS are denied so that an actual memory access does not take place. As a result it is possible therefore to refresh an unlimited quantity of memory cards at once, with the same refresh signals. (The refresh address was originally produced by the Z80-CPU itself, but as it is only 7 bits, (ie AB0-AB6) it is likely that some modification will be required to the refresh arrangements if 256K DRAM chips are used (since these need more than a 7 bits refresh).)

21A NRST System Reset (Open Collector to or from CPU/Controller)

This signal is active (ie low) when the reset switch on the CPU card is reset. It is used to reset circuitry on all of the cards in the system which require such a signal. If the reset line is brought low by the action of a device other than the CPU then the CPU is also reset. The line is normally held high by a 1k pull-up resistor on the CPU card.

(The Kemitron MZB-3 CPU card does not comply with this specification in all details.)

So as not to run the risk of damage to data in the dynamic RAMs when the reset switch is operated, the CPU card produces a short duration pulse rather than a permanent signal for the duration of the reset switch operation. Furthermore the start of the pulsed refresh is arranged to be never during a memory access (because an incompleted access could corrupt a row of data in a dynamic RAM).

22A-29A DB7-DB0 8-bit Data Bus (Bidirectional, 3-state)

These are the data lines used for 8-bit bidirectional data exchanges between the CPU or Controller and Memory or Input/Output Cards. Positive logic is used (as for the address lines previously described). In 8-bit systems these 8 lines are the only 8, but for systems using a 16-bit bus there are a further 8 lines defined on the "B" side of the bus.

30A (Unallocated) Daisy Chain 1 In (Daisy Chain TTL Level Input)
31A (Unallocated) Daisy Chain 1 Out (Daisy Chain TTL Level Output)

These two lines allow an additional and as yet unallocated priority daisy chain to be set up. Viewed from the plug in card side of the edge connector, the output of the card on the left is connected to the input of the card on the right. The convention used will be active low.

32A NRFSH DRAM Refresh (TTL Level Output from CPU/Controller)

Refresh line, active low, indicates that the lower address bus lines (at least the seven lines AB0-AB6, but may be more) hold a refresh address for dynamic RAMs. It is the duty of the CPU or Controller card to ensure that refresh addresses are issued frequently enough for proper refresh of dynamic RAMs in the system. If the dynamic RAM card in use has its own refresh counter the CPU or Controller is relieved of this duty; the NRFSH signal can then merely be used to signal to the dynamic RAM card that now is an appropriate time for a refresh to take place.

33A CLK MPU Clock (TTL Level Output from CPU/Controller)

This is the single phase system clock (often 2.5 MHz for a standard Z80-CPU, 4 MHz for the "A" version, 6 MHz for the "B" version and 7.5 MHz for the "H" version). Ø is derived from the 2 x MPU clock to be found at pin 34B of the ISBUS. Ø changes state on the negative transition of 2Ø. The buffering on the CPU card should be organised so that the bus clocks Ø and 2Ø are one buffer delay in advance of the CPU clock itself. This is because (in the case of a Z80 system) many of the family peripheral chips cannot accept a TTL Level clock: its voltage swing and current drive have to be amplified first, which adds an extra buffer delay.

34A NWAIT Wait State Request (Open Collector Input to CPU/Controller)

This signal, if active (ie low) during the Z80 "T2" time, indicates that an addressed device requires "wait" states to be inserted into the current Memory or I/O cycle. This is usually to accommodate slow devices which require an increased time before data can be provided or taken, but another use for "wait" states is to allow synchronisation between the CPU and the Memory or I/O device if timing is critical (e.g. for some floppy disk controllers, or VDU designs). If the CPU is providing dynamic RAM refresh, prolonged use of "wait" states should be avoided as it may predjudice proper refreshing of the dynamic RAM. (There is no need to panic on this point - the maximum wait state allowed can be calculated fairly easily for specific cases.) A 1k pull-up resistor is fitted on the CPU card.

35A +12V +12V Power Supply Rail
36A +12V +12V Power Supply Rail

Together with their "opposite numbers" 35B and 36B on the other side of the connector, these are the conductors of +12V regulated d.c. power from the power supply to the system. Generally these rails carry no more than an Ampere or two, and if this is the case there is no need to reinforce the copper track on the bus board.

37A Pol Polarisation Slot

This line is not available for signals as this position is removed for polarisation. An important secondary purpose for the polarisation key fitted in each connector at this position is to pull the cards into line - to prevent individual connectors shorting between adjacent contacts.

38A -12V -12V Power Supply Rail
39A -12V -12V Power Supply Rail

Together with 38B and 39B on the other side of the connector, these are the conductors of -12V regulated d.c. power from the power supply to the system. Generally these rails carry much less than an Ampere, and if so there is no need to reinforce the copper track on the bus board.

40A 0V 0V Power Supply Rail
41A 0V 0V Power Supply Rail

Together with 40B and 41B on the other side of the connector, these provide the return path to 0V and Earth for the currents flowing in the +12V, +5V and -12V rails. Usually the algebraic sum of these currents is more than the absolute value of any one of them, so these rails carry most current of all. If the current is substantial, say 10 Amperes or more, it may be advisable to reinforce these rails with lengths of heavy gauge tinned copper wire e.g. 18 swg. This is quite easy to do because the wire can lie between the two adjacent rails provided for this voltage on each side of the connector.

42A +5V +5V Power Supply Rail
43A +5V +5V Power Supply Rail

Together with 42B and 43B on the other side of the connector, these are the conductors of +5V regulated d.c. power from the power supply to the system. If the current drawn from this rail is substantial, say approaching 10 Amperes or more, it may be advisable to reinforce these rails with lengths of heavy gauge tinned copper wire e.g. 18 swg. This is quite easy to do because the wire can lie between the two adjacent rails provided for this voltage on each side of the connector.

This concludes the description of the signals on the "A" side of the ISBUS. These are all that have been used so far and alone they permit a very powerful system (which has stood the test of time) to be implemented. However as developments in computers proceed there may come a time when even more capability is required. The as yet unused "B" side connectors have been provided for future enhancements which therefore will be possible without the need to scrap all that has been

built so far. If the Interak system is compared with its contemporaries (ie systems designed 5 or 6 years ago) it will be seen how far-sighted this approach has been. The vast majority of earlier computers have had to be scrapped once the limits of 8 bits and 64K have been reached, and it is intended that this will not be the fate of the Interak system.

The following pages describe these extra "B" side signals.

"B" Side Connectors

1B NEIOREQ Extended I/O Request (TTL Level Output from CPU/Controller)

This is an active low signal which is only used in systems with a 64K I/O space (i.e. 16-bit Port Address Bus). It has a similar function to the NIOREQ line on 1A of the bus, but NEIOREQ is only issued when the extended port space is brought into play.

2B NEMREQ Extended Memory Req (TTL Level Output from CPU/Controller)

This is a signal (active low) which is only used in systems with a 16 Megabyte Memory Space (i.e. 24-bit Address Bus). It has a similar function to the NMREQ line on 1B of the bus, but NEMREQ is only issued when the extended address space is to be used.

3B NADS Address Strobe (TTL Level Output from CPU/Controller)

This is an active low signal which has been allocated for future use. Once 32-bit (and beyond?) CPUs are introduced, the idea of separate address and data buses (i.e. 32+32=64 bits) becomes unwieldy; it is possible that the normal implementation will be to use a multiplexed address-data bus. As ISBUS has 16 data bus lines defined, and 24 address bus lines, i.e. 16+24 = 40 lines in total this will be more than enough for 32-bits. When this happens, an extra strobe will be required: NADS, which indicates that the address-data bus holds a 32-bit address. When NADS is over the bus will then be driven with the data corresponding to that address.

The possibility of non-multiplexed 32-bit address and data buses has not been ruled out, but if they are introduced this will need very extensive alterations to the bus signals. Indeed so much will have to change that the user may then have to say goodbye to the old cards forever. A better idea in our view, if a lot of investment has been made in non 64 address and data bit systems, is that then more than one CPU be run simultaneously, on separate buses, sharing the computational load between each other.

4B NDIRIN Direction In (to MPU) (TTL Level Output from CPU/Controller)

It is very convenient for setting buffer directions if the CPU/Controller card issues a direction signal early in its cycle. Most current CPUs do not issue such a signal, but if in the future CPUs etc. are used which do, this bus line has been allocated to carry it. It is an active low signal.

5B NM1(OCF) M1 (Opcode Fetch) (TTL Level Output from CPU/Controller)

This is the M1 signal from the Z80 CPU. It is used to indicate that the CPU is fetching an op-code. (M1 is also asserted by the CPU with -IORQ during the special conditions of an interrupt acknowledge cycle.)

6B (Unallocated) Extended Signal 1 (TTL Level Output from CPU/Controller)

7B (Unallocated) Extended Signal 2 (TTL Level Output from CPU/Controller)

Although it is an irritating feature of a bus standard to have unallocated lines, these are so at present. They should not be employed for the user's own purposes, as this may conflict with whatever signal is allocated to them in the future. If they carry control signals the signals will be active low.

8B NZCMAINS Zero Crossing (Mains) (TTL Level Output from CPU/Controller)

This signal is a series of short pulses (active low), synchronised with the zero crossings of the ac mains input to the computer. It has three main purposes - firstly for triggering ac power controlling devices and the like (so that ac powered circuits can be switched on only when the mains voltage is passing through zero thus avoiding current surges and unwanted generation of electromagnetic interference) - secondly to provide advance warning of an imminent power failure (since when the ac mains fails there will be a period of continuous "zero crossing" before dc power fails) - and finally to offer a simple timing pulse of known repetition frequency which is independent of any software (this can be used for example to set a "watchdog" timer to alert of or restart a "looping" or "crashed" program).

9B NNMI Non Maskable Interrupt (Open Collector to or from CPU/Controller)

Active low, non-maskable interrupt line. 1k pull-up resistor fitted on the CPU card.

10B NINTA Interrupt A (Open Collector to or from CPU/Controller)

Active low, maskable interrupt line, 1K pull-up resistor fitted on the CPU card.

11B NINTB Interrupt B (Open Collector to or from CPU/Controller)

This is a further active low line similar in function to Interrupt A and is provided for any future CPUs which can use an extra interrupt line.

12B NINTC Interrupt C (Open Collector to or from CPU/Controller)

This is a further active low line similar in function to Interrupt A and is provided for any future CPUs which can use an extra interrupt line.

13B-20B AB16-AB23 Extended Address Bus (TTL Level Output from CPU/Controller)

These provide an extra 8 positive logic address lines to extend the memory space memory space to 16 Megabytes. The extra lines are produced by the CPU/Controller card. When these lines are used in a system the NEMREQ (Extended Memory Request) signal replaces the ordinary NMREQ signal of a non-extended (64K) system, to prevent any conflict where the old 64K system memory space is shared with the new 16 Megabyte system.

21B NBUSREQ Bus Request (Open Collector Input to CPU/Controller)

This is an active low signal which is output by some card (e.g. Direct Memory Access Controller) to request the existing controller (e.g. CPU card) to relinquish its control of the bus. Most of the bus output lines from the existing controller are allowed to go tri-state, and it then generates the signal NBUSAK (q.v.) Care must be taken when using this technique to ensure that arrangements for dynamic RAM refresh (for example) are properly made if the CPU card is effectively switched off.

(At the time of writing no decision has been taken on whether or not the clock signals generated by the CPU card should also be rendered tri-state, and replaced by ones from the DMA controller, also the question of what effect interrupts should have is likewise very vague.)

22B-29B DB15-DB8 Extended Data Bus (Bidirectional, 3-state)

When systems require a 16-bit data bus, these lines carry the upper 8-bits of that data. They are directly opposite the bus lines for the lower 8-bits and this enables easy conversion of existing 8-bit cards to use the uppper 8-bits instead, so that cards can be used in pairs to provide an easy upgrade to 16-bits. The positive logic convention is used, as described for the address lines on the "A" side.

30B NIEI Interrupt A Daisy In (Daisy Chain TTL Level Input)
31B NIEO Interrupt A Daisy Out (Daisy Chain TTL Level Output)

These active low signals are used by Z80 peripherals to form an interrupt daisy-chain for determination of interrupt priority. This is done in accordance with the rules set out by the manufacturers of the chips to be used.

32B NBAI Bus Available Daisy In (Daisy Chain TTL Level Input)

This active low signal forms a daisy chain with NBAO (below). The action is for a slave device/channel controller not to start an access if this line is high.

33B NBAO Bus Available Daisy Out (Daisy Chain TTL Level Output)

This active low signal forms a daisy chain with BAI. It is set low by e.g. the CPU card when the CPU has received a request from say a Direct Memory Access controller to release the system bus. NBAO is high when the bus is being used.

Because it is part of a daisy chain, the physical order of the cards using it will determine their priority to access the bus.

34B 2XCLK 2 x MPU Clock (TTL Level Output from CPU/Controller)

This is a clock of twice the frequency of that on bus line 33A (and thus is often 5 MHz for a standard Z80-CPU, 8 MHz for the "A" version, 12 MHz for the "B" version and 15 MHz for the "H" version). Ø on pin 33A is derived from this clock; Ø changes state on the negative transition of 2Ø. The buffering on the CPU card should be organised so that the bus clocks Ø and 2Ø are one buffer delay in advance of the CPU clock itself. This is because (in a Z80 system) many of the family peripheral chips cannot accept a TTL Level clock: its voltage swing and current drive have to be amplified first, which adds an extra buffer delay.

35B +12V +12V Power Supply Rail
36B +12V +12V Power Supply Rail

These are connected to the same +12V Power Supply Rail as described for connections 35A and 36A on the "A" side of the connector.

37B Pol Polarisation Slot -

This line is not available for signals as this position is removed for polarisation. Also it is used with the key fitted in each connector to pull the cards into line and prevent individual connectors shorting between adjacent contacts.

38B -12V -12V Power Supply Rail
39B -12V -12V Power Supply Rail

These are connected to the -12V Power Supply Rail - see the description for connections 38A and 39A on the "A" side.

40B 0V 0V Power Supply Rail
41B 0V 0V Power Supply Rail

The 0V Rail is on these two pins, and the 40A and 41A on the "A" side. See the description for 40A and 41B for full details.

42B +5V +5V Power Supply Rail
43B +5V +5V Power Supply Rail

These, and 42A and 43A on the other side of the connector form the +5V Power Supply Rail. See the description for 42A and 42B for more information.

Derived_Signal

NINTAK: This signal indicates that the CPU is acknowledging an interrupt and expects an interrupt vector to be placed on the data bus.

The NINTAK signal can be produced as the output of an "OR" gate (e.g. 74LS32) which has NIOREQ and NM1(OCF) connected to its inputs. As it can be produced in this way anywhere it is needed there is no need to allocate a bus line to it.

E & OE January 1985

Construction Notes for ISBUS-2

1. Read all documents carefully before starting.

2. If you have a continuity tester, test the ISBUS bare board for short circuits. In the unlikely event that any shorts are found it is much easier to clear them on the bare board than when the connectors are fitted.

3. The board has sides 'A' and 'B' marked both 'in copper' and on the 'Component Ident'. Side 'A' has all the parallel signal tracks running the length of the board and is marked with power connector positions JA1 to 13. Side 'B' has 'Earth' screening and reinforcement of the 0V and +5V tracks,and is marked with the edge connector positions JB1 to JB13. The edge connectors are fitted on the 'B' side and soldered on the 'A' side, the power connectors are fitted on the 'A' side and soldered on the 'B' side. The unused power connector positions should be used to bond 'A' and 'B' sides together so that the power is passed from the power connectors to the power rails on the 'A' side and to reinforce the +5 volt and 0 volt rails.

4. The board can be used with single or double edge connectors, although double connectors are used more frequently as ironically they are often cheaper. The "wire wrap" type should be used, as the types with solder tags will not fit through the 1.0 mm holes provided. Proper printed circuit board mounting types can of course be used equally well, but the wire wrap termination types make testing, repairs and modifications much easier. (See **** for additional points to consider when choosing connectors.)

5. As ISBUS is substantially a "parallel" bus (i.e the "any card in any slot" type - but with some reservations) it can only be used to interconnect cards which suit it. All "Interak" cards will suit, most "Kemitron" cards (with minor alterations), but some early "Kemitron" cards will not; in particular the Kemitron VDU-A,B,G 3-card set, (effectively replaced by the Interak VDU-K and VDU-2K), and the Kemitron DCR-6 Keyboard interface of the (effectively replaced by the Interak LKP-1). There were few of these cards sold by Kemitron, Crofton, March Communications and others, and that was several years ago (circa 1979), so further discussion on this topic is not merited (contact your supplier for advice if you think it is).

6. ISBUS can accommodate up to 13 connectors, but they do not all need to be fitted at the same time. However, no matter how many are to be fitted the following procedures should be followed.

7. Before fitting any connectors the 'A' and 'B' sides should electrically bonded. This is done by soldering short pieces of thick gauge wire through the holes which will not be filled with power connectors later (ie leave connector positions JA3, JA7, JA11 vacant). Use a large size soldering iron bit and also a more powerful soldering iron if available. Cut the thick tinned

copper wire into pieces approximately 35mm long and form these into 'U' shapes so that they will fit into adjacent holes which require bonding. By forming the wire in this way it allows the joint to be made with less risk of the wire falling out or moving and making a bad joint. It also allows the joint to be rechecked as the excess wire is being trimmed off. A tool which is very useful for trimming the thick wire is called the 'microshear'. If you de-flux your boards now is a good time to clean up the 'B' side as it will be more difficult when the edge connectors are fitted.

8. Loosely fit all the edge connectors, but do not solder yet. Before you begin ensure that the connectors are in perfect condition - it will be difficult to remove a damaged connector later, after it has been soldered.

9. The polarising key in some types of connectors will hold the board "proud" at one end, and we suggest purely for neatness' sake that a similar gap be left at the other end:

10. At the next step leave space for the 3.5" disk drives next to connector 13, i.e. bias the ISBUS so that slot 1 is close to the left-hand side of the rack when viewed from the front.

11. The ISBUS is fixed in the 19" card frame by means of the fixing feet on each connector. All of the connectors should be securely screwed into the card frame so that they take the force when cards are plugged in and withdrawn, not the ISBUS board.

12. Before soldering, screw all of the connectors into the card frame and plug in as many cards as you can. It is far easier to correct any slight errors in assembly at this stage than it is after the soldering is complete.

13. With the boards still in position, and the ISBUS board positioned neatly as described in section 7 above, solder a few connections at both ends of each connector. Be as quick as you can, because if you apply too much heat the track may lift on the circuit board which is plugged in, which would render it useless - the quality of the joint is not important at this stage, you can always return to it later when the plug in board has been safely removed.

14. Check by removing the plug in cards and reinserting them that everything has been correctly assembled. (The cards should be exactly in line with the connectors so that the contacts exert equal pressure on both sides. With a new set of connectors, and particularly if you have forgotten to chamfer and lubricate the edge connectors, a lot of force may be needed to insert a card - ensure that this is not the result of any mechanical misalignment or obstruction).

15. Leave the cards out and complete the soldering, not forgetting to return to the first few joints which were made in haste at an earlier stage in the proceedings.

16. If you prefer you can remove the ISBUS assembly from the card frame, but take great care to maintain correct alignment of the edge connectors. This can be done by undoing one of the connector mounting rails and sliding the end feet off all the edge connectors, leaving the end feet bolted to the mounting rail. The ISBUS board complete with connectors can likewise be removed from the other connector mounting rail. It's a bit fiddley but the only other alternative is to undo all of the connector retaining nuts individually.

17. Solder the connector pins to the ISBUS giving attention to the following points:

(i) Use a clean fine-tipped soldering-iron.

(ii) Wet the tip of the soldering-iron with a small amount of solder (but not enough to form a 'blob').

(iii) Place the tip of the soldering-iron bit on the junction between the connector pin and the circuit board track. At most positions there is a lager area or "land" to one side of the hole - this is for the soldering iron. (Do not press hard as excessive pressure can damage the board.)

(iv) After a few moments push a few millimetres of thin rosin flux cored solder into the junction between the circuit board track and the connector pin (not onto the soldering-iron). The solder will melt and run into the junction of the connector pin and the track. Use sufficient solder to flow all round the connector pin so far as is possible. Owing to the build up of tolerances where the green solder resist mask is registered on the track pattern it may not be possible to satisfy this last requirement completely. Remove the soldering-iron from the joint, trying not to run up the length of the wire-wrap pin, as the pins may be used in the future for wire-wrapped modifications or expansion via push fit ribbon cable connectors. The surface of the solder should be concave when the soldering iron is removed. If the solder forms a large bump where the soldering iron has been, either the joint was not hot enough, or the soldering iron was left on the joint too long after the solder was applied, or of course you may have applied too much solder.

(v) Inspect the joint. If it looks unsightly, or if the solder has not flowed properly, the joint should be re-heated and a very small amount of solder applied (again not to the soldering-iron), and the soldering-iron removed. If after this the joint is still unsatisfactory, a solder sucking pump or de-soldering braid should be used to remove the solder, as all the original flux will have been burnt off, and it will be worthwhile starting again at 11 (i) above.

When moving quickly from one joint to the next there will be no need to wet the iron again between joints. If a joint is unsatisfactory resolder it immediately. Do not leave it to the end as you may forget to go back, and a lot of time consuming fault-finding diagnosis may be required just to find the faulty joint once it has been forgotten.

Stop soldering if blobs of flux form on the iron or joints, and clean the bit on a damp sponge or cloth, start at step 12 (i) when resuming.

If you short across any tracks with a solder bridge, stop soldering and clear the short immediately using de-soldering braid or a solder sucker.

18. Do not get excess solder along the length of the wire wrapping pins: they may be required later for wire wrapped modifications, or for later expansion via push fit ribbon cable connectors, or for push fit termination networks for experimental use.

19. If you de-flux your circuit boards now is an ideal time to clean the 'A' side.

20. Ensure that there are still no shorts between tracks and that all tracks are continuous. The use of a simple continuity tester to detect open and short circuits, and the time taken, will be amply repaid if a fault is found at this stage rather than later when a number of expensive boards have been plugged into the system.

21. Fit the three power connectors from the 'A' side and solder on the 'B' side. It is best if you solder just one pin of each connector then check that it has been correctly fitted before soldering the rest. If available use a more powerful soldering iron fitted with a larger bit as mentioned above for the through links.

22. If you removed the ISBUS card refit it onto the card frame taking great care that the edge connectors line up with the plug in cards. Plug in as many cards as you can before finally tightening the edge connector fixings.

23. Connect the standard power supply lead (if used). The two 5 way connectors which supply +5 volts (red wire) and 0 volts (green wire) in them should be plugged onto the connectors at positions

'JA3' and 'JA11', and the remaining 5 way connector which has three wires +12 volts (orange wire) -12 volts (black wire) and 0 volts (green wire) should be plugged onto the connector at position 'JA7'. The 12 way connector which remains will be connected to the PSD-1 board later when it is fitted. As the wires are of fairly heavy gauge take care to arrange them so that they are not damaged by the edge connector wire-wrap pins or trapped between other metal work.

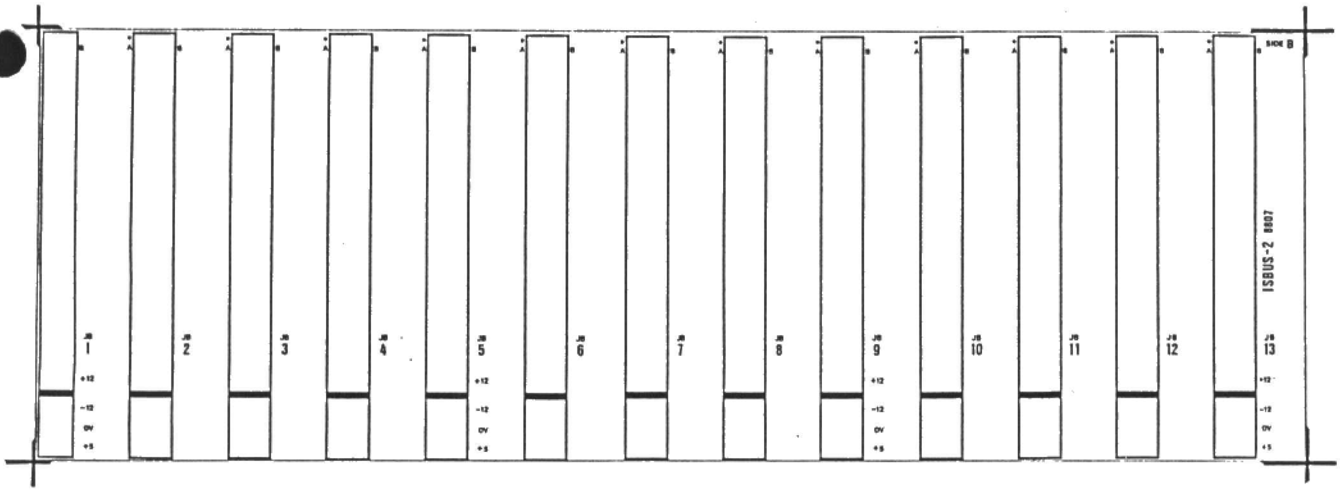
25. Remove all the assembled plug in cards. If using a switch-mode power supply of the type which requires certain minimum loads connect suitable loads. If you are making several systems it may suit your convenience to make up a plug in board (e.g. DIP-1) which will serve as a connection point for the dummy loads. Switch on the power and measure the voltages on the back board between earth and the other power supply rails. If they are within the limits laid down in the PSU data, remove the dummy loads if necessary and plug in the cards to be used. Follow the general rule that memory using cards should close to the CPU, and I/O (Input/Output) card can be further away. In an extensive system the cards will have to be placed in a suitable order to establish any desired interrupt and other daisy-chain priorities.

ISBUS-1 BUS ALLOCATIONS

No.	Name	Type	Signal Description	No.	Name	Type	Signal Description
1A	NIOREQ	(1)	I/O Request	1B	NEIOREQ	(1)	Extended I/O Request
2A	NMREQ	(1)	Memory Request	2B	NEMREQ	(1)	Extended Memory Request
3A	NWDS	(1)	Write Data Strobe	3B	NADS	(1)	Address Strobe
4A	NRDS	(1)	Read Data Strobe	4B	NDIRIN	(1)	Direction In (to MPU)
5A	AB15	(1)	Address Bus 15	5B	NM1(OCF)	(1)	M1 (Opcode Fetch)
6A	AB14	(1)	Address Bus 14	6B	-*-	(1)	Extended Signal 1
7A	AB13	(1)	Address Bus 13	7B	-*-	(1)	Extended Signal 2
8A	AB12	(1)	Address Bus 12	8B	NZCMAINS	(1)	Zero Crossing (Mains)
9A	AB11	(1)	Address Bus 11	9B	NNMI	(O)	Non Maskable Interrupt
10A	AB10	(1)	Address Bus 10	10B	NINTA	(O)	Interrupt A
11A	AB9	(1)	Address Bus 9	11B	NINTB	(O)	Interrupt B
12A	AB8	(1)	Address Bus 8	12B	NINTC	(O)	Interrupt C
13A	AB7	(1)	Address Bus 7	13B	AB23	(1)	Extended Address Bus 23
14A	AB6	(1)	Address Bus 6	14B	AB22	(1)	Extended Address Bus 22
15A	AB5	(1)	Address Bus 5	15B	AB21	(1)	Extended Address Bus 21
16A	AB4	(1)	Address Bus 4	16B	AB20	(1)	Extended Address Bus 20
17A	AB3	(1)	Address Bus 3	17B	AB19	(1)	Extended Address Bus 19
18A	AB2	(1)	Address Bus 2	18B	AB18	(1)	Extended Address Bus 18
19A	AB1	(1)	Address Bus 1	19B	AB17	(1)	Extended Address Bus 17
20A	AB0	(1)	Address Bus 0	20B	AB16	(1)	Extended Address Bus 16
21A	NRST	(O)	System Reset	21B	NBUSREQ	(O)	Bus Request
22A	DB7	(2)	Data Bus 7	22B	DB15	(2)	Extended Data Bus 15
23A	DB6	(2)	Data Bus 6	23B	DB14	(2)	Extended Data Bus 14
24A	DB5	(2)	Data Bus 5	24B	DB13	(2)	Extended Data Bus 13
25A	DB4	(2)	Data Bus 4	25B	DB12	(2)	Extended Data Bus 12
26A	DB3	(2)	Data Bus 3	26B	DB11	(2)	Extended Data Bus 11
27A	DB2	(2)	Data Bus 2	27B	DB10	(2)	Extended Data Bus 10
28A	DB1	(2)	Data Bus 1	28B	DB9	(2)	Extended Data Bus 9
29A	DB0	(2)	Data Bus 0	29B	DB8	(2)	Extended Data Bus 8
30A	-*-	(D)	Daisy Chain 1 In	30B	NIEI	(D)	Interrupt A Daisy In
31A	-*-	(D)	Daisy Chain 1 Out	31B	NIEO	(D)	Interrupt A Daisy Out
32A	NRFSH	(1)	DRAM Refresh	32B	NBAI	(D)	Bus Available Daisy In
33A	CLK	(1)	MPU Clock	33B	NBAO	(D)	Bus Available Daisy Out
34A	NWAIT	(O)	Wait State Request	34B	2	(1)	2 x MPU Clock
35A	+12V	(P)	+12V Power Supply	35B	+12V	(P)	+12V Power Supply
36A	+12V	(P)	+12V Power Supply	36B	+12V	(P)	+12V Power Supply
37A	Pol	-	Polarisation Slot	37B	Pol	-	Polarisation Slot
38A	-12V	(P)	-12V Power Supply	38B	-12V	(P)	-12V Power Supply
39A	-12V	(P)	-12V Power Supply	39B	-12V	(P)	-12V Power Supply
40A	0V	(P)	0V Power Supply	40B	0V	(P)	0V Power Supply
41A	0V	(P)	0V Power Supply	41B	0V	(P)	0V Power Supply
42A	+5V	(P)	+5V Power Supply	42B	+5V	(P)	+5V Power Supply
43A	+5V	(P)	+5V Power Supply	43B	+5V	(P)	+5V Power Supply

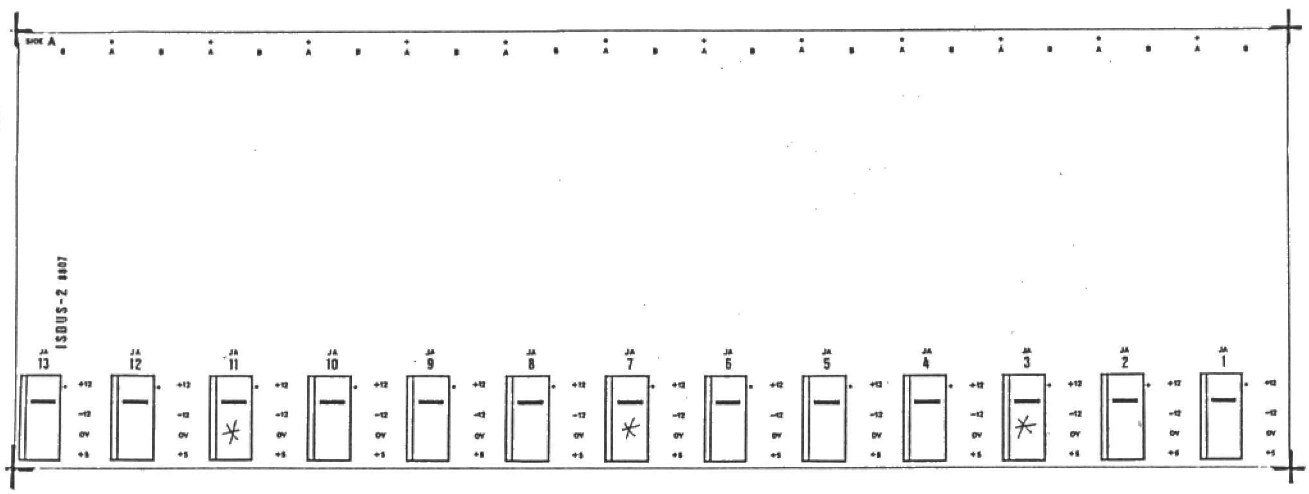
"-*-" = Unallocated; "O" = Open Collector; "1" = Unidirectional Bus;
"2" = Bidirectional Bus; "D" = Daisy Chain In/Out; "P" = Power Supply.

(The KBUS-12 allocations used for some "Kemitron" cards are substantially the same, except that the NWAIT line is on A30, the signal on A31 is designated "spare", and the NRST line on A21 is a TTL totem pole output not open-collector. The KBUS-5 allocations used on some other "Kemitron" cards are the same as for KBUS-12, except that the voltage rail on A38 and A38 is -5V not -12V. For consistency and safety, the Interak 1 uses the one bus standard throughout, namely the ISBUS-A, as listed above.)



FIT EDGE CONNECTORS FROM THIS SIDE SOLDER ON A SIDE

Drawn JHP	**Greenbank Electronics**	
Date 10-10-88	ISBUS-2 SIDE B	
Scale N.T.S.	COMPONENT IDENT	



* FIT POWER CONNECTORS FROM THIS SIDE AT POSITIONS 11, 7, 3
SOLDER ON 'B' SIDE.

Drawn JHP.	**Greenbank Electronics**	
Date 10-10-88.	ISBUS-2 SIDE 'A'	
Scale N.T.S.	COMPONENT IDENT	

COMPONENT PARTS LIST FOR ISBUS-2

Issue 1. Date: October 1988

List by Component Reference Number.

Connectors		Order Code
JB1	43 Way Double-sided Interak Edge Connector	43DS
JB2	43 Way Double-sided Interak Edge Connector	43DS
JB3	43 Way Double-sided Interak Edge Connector	43DS
JB4	43 Way Double-sided Interak Edge Connector	43DS
JB5	43 Way Double-sided Interak Edge Connector	43DS
JB6	43 Way Double-sided Interak Edge Connector	43DS
JB13	43 Way Double-sided Interak Edge Connector	43DS
JA3	0.156" 5 Way Polarised Plug Straight Friction Lock	PL156S5P
JA7	0.156" 5 Way Polarised Plug Straight Friction Lock	PL156S5P
JA11	0.156" 5 Way Polarised Plug Straight Friction Lock	PL156S5P

Sundries

16swg	Tinned Copper Wire approximately 750mm Long. (For 'Thru' links to bond 'A' side to 'B' side.)	TCW16750

List by Component Type.

43DS	7	JB1-6,13
PL156S5P	3	JA3,7,11
TCW16750	1	For 'Thru' links to bond 'A' side to 'B' side.

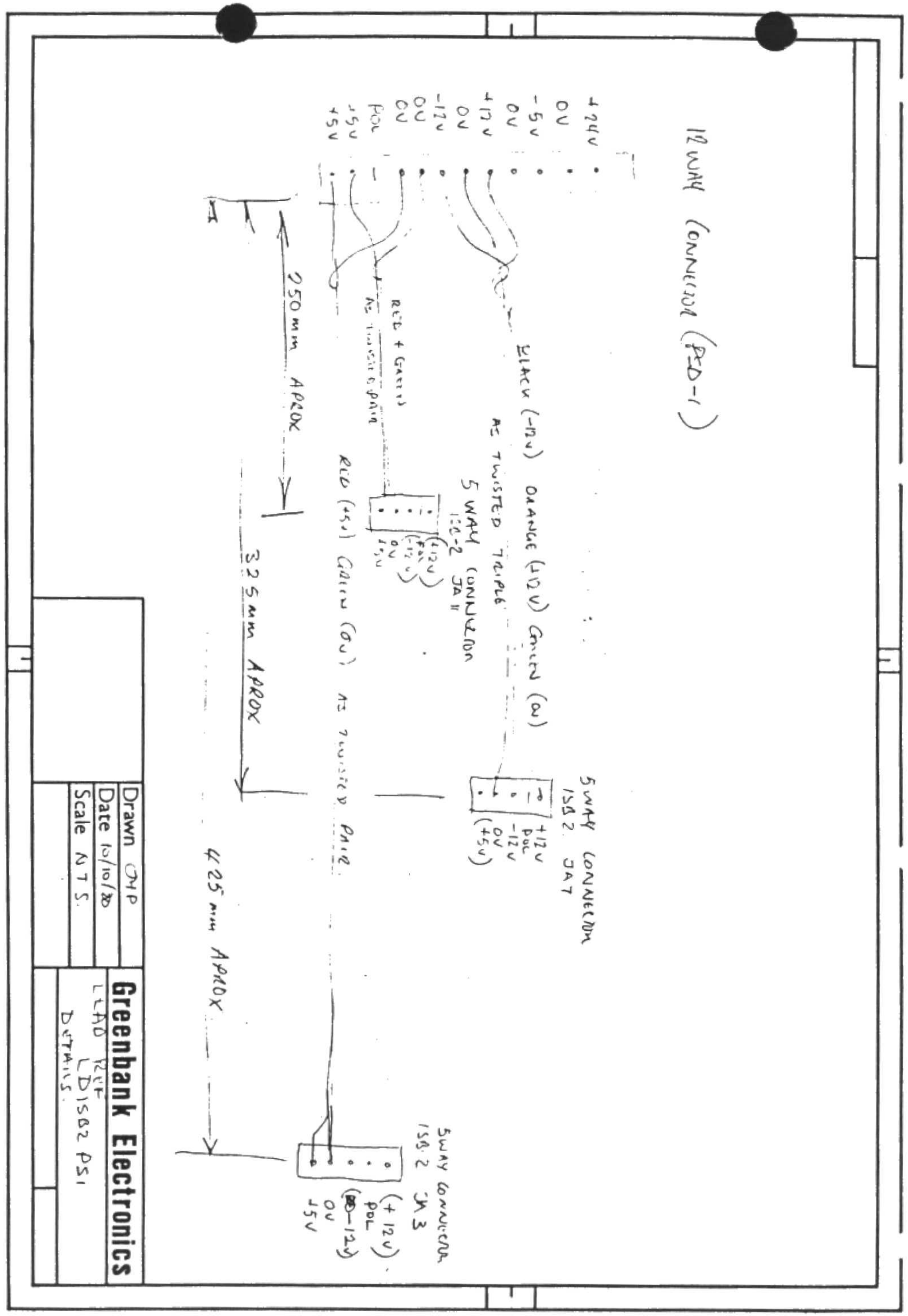
Optional Extras.(i.e. Items not included in standard kit of parts)

ISBUS p.c.b, sold separately as "BISB2" Bare Board		BISB2
Manual, sold separately as "MISB2" (Zero Rated for VAT)		MISB2
Interak Edge Connector (43-way Double Sided) (each)		43DS
Mounting Brackets or "End Feet" (already included in the above)	(each)	ECFEET
Edge connector Fixings	(Per 10)	HEX1

* These items are also contained in a kit of parts and are more fully detailed in the PSD-1 manual (power supply distribution board).

* ISBUS-2 dc Power Lead Standard 'Made Up'	LDISB2PS1
* 0.156" connectors and sundries	
* 5 way Str/Fr Lock Polarised	PL156S5P
* (Polarising Key available separately see below)	
* Shell 5 way (SBC-1, ISB-2 Power connector)	SH1565
* Shell 12 way (PSD-1 DC Power)	SH15612
* 0.156" Polarising Key #1	POLK1561
* 0.156" Crimp Large (suit wire 24/0.2-32/0.2)	CRMP156L

-5



Prices each, ex.VAT

Connectors

Up to 13 edge-connectors may be fitted. The number fitted will be at your discretion and obviously fitting all 13 edge connectors at the outset is wisest if funds permit. We have selected 7 connectors as being the contents in a kit because this is the reasonable minimum quantity which would be required. As with all Interak kits all parts are available separately so if your application requires only part of a kit just order the parts you want.

The connectors are described as being 43-way, but pin 37 has been removed and replaced with a polarisation key, so in reality there are only 42 connection ways. To follow the convention set by connector manufacturers we describe the double sided type (ie the only type we supply) as 43-way double sided, although in fact it has 84 ways. The connectors have "wire wrap" terminations, even though they are to be soldered to the ISBUS board. (This termination style has been chosen to allow discrete wire repairs to be made to an ISBUS board should it become damaged: owing to the large number of very closely spaced thin tracks, rectification of damage on the board or replacement of damaged connectors cannot be carried out satisfactorily on the ISBUS board itself.)

The connector price includes two metal mounting brackets or "feet", but you can buy them separately to suit your convenience if you purchase your connectors elsewhere. (If you do, make sure that you buy connectors which suit the metal mounting brackets; if the types with plastic end feet are purchased the feet obstruct the connectors so that the boards will not plug in without being filed to fit. Also do take care that you buy good quality connectors like ours - you have to trust your supplier on this point as a poor quality connector looks very similar to a top quality one. The difference is in the type of plastic used for the body, dimensional stability, contact construction, material and plating and so on.)

Hint: For the most reliable installation and maximum lifetime, always use a very fine file to chamfer the plug-in edges of the cards to provide a smooth "lead in", and use an appropriate lubricant. (This topic is discussed further in most of the individual card manuals.)

The method of fixing the connectors into the rack varies. We supply packs of "edge connector fixings" (ie appropriately sized hexagonal headed bolts and nuts) to suit our type of rack. They are listed in our hardware leaflet, but they are mentioned again below simply as a reminder that they are needed.

Connectors and Sundries

43DS	7	JB1-6,13	3.95	27.65	
PL156S5P	3	JA3,7,11	0.40	1.20	
TCW16750	1	FOR 'Thru' links to bond 'A' side to 'B' side at vacant connector positions JA1,2,4-6,8-10,12,13	0.30	0.30	
	11	Total cost of kit of all parts listed so far PISB2:		29.15	29.15

OPTIONS (i.e. Items not included in standard kit of parts)

ISBUS p.c.b, sold separately as "BISB2" Bare Board		BISB2	13.50
Manual, sold separately as "MISB2" (Zero Rated for VAT)		MISB2	1.00 0%
Interak Edge Connector (43-way Double Sided)	(each)	43DS	3.95
Mounting Brackets or "End Feet" (already included in the above price)	(each)	ECFEET	0.25
Edge connector Fixings	(Per 10)	HEX1	0.64

* These items are also contained in a kit of parts and are more fully detailed in the PSD-1 manual (power supply distribution board).

* ISBUS-2 dc Power Lead Standard 'Made Up'	LDISB2PS1	2.50
* 0.156" connectors and sundries		
* 5 way Str/Fr Lock Polarised	PL156S5P	0.40
* (Polarising Key available separately see below)		
* Shell 5 way (SBC-1, ISB-2 Power connector)	SH1565	0.20
* Shell 12 way (PSD-1 DC Power)	SH15612	0.31
* 0.156" Polarising Key #1	POLK1561	0.07
* 0.156" Crimp Large (suit wire 24/0.2-32/0.2)	CRMP156L	0.03

(Add 50p handling charge to each transaction, and 15% VAT.)

Greenbank Electronics
460 New Chester Road
Rock Ferry, Birkenhead
Merseyside. L42 3AE
Telephone:-051-645 3391

Access and Visa Welcome (no surcharges).